NVRAM for the computer scientist

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A computer

CPU

DRAM

Disk

Access time: 50 ns
Loose data when not powered

Access time: 100000 ns
Retains data when not powered
A computer

Access time: 50ns
Loose data when not powered
A computer

- CPU
- DRAM
- Disk

**Access time**: 50ns  
Loose data when not powered

**Access time**: 100000 ns  
Retains data when not powered
NVRAMs

Read/Write times, scalability, density, energy consumption
NVRAMs

Read/Write times, scalability, density, energy consumption

PCM
- Read time: 100 ns
- Write time: 200 ns
NVRAMs

Read/Write times, scalability, density, energy consumption

MRAM
- Read time: 10ns
- Write time: 20ns
NVRAM for mass storage
NVRAM for mass storage
NVRAM for mass storage

- Dedicated file systems
- Database in NVRAM
DRAM + NVRAM

- CPU
- DRAM
- Disk

- DRAM + PCM: More RAM
- DRAM + PCM: Wear-Leveling
DRAM + NVRAM
DRAM + NVRAM

- DRAM + PCM: More RAM
- DRAM + PCM: wear-Leveling
- ...

CPU

NVRAM

DRAM

Disk
Architecture

- CPU
- DRAM
- Disk

▶ 4x more, 2x slower ?
▶ L1 ? L2 ? L3 ?
▶ Several technologies ?
Architecture

- CPU
- Disk
- DRAM
- L1 Cache
- L2 Cache

▶ 4x more, 2x slower?
▶ L1 ? L2 ? L3 ?
▶ Several technologies?
Architecture

- 4x more, 2x slower?
- L1 ? L2 ? L3?
- Several technologies?
NVRAM as working memory

Existing works with PCM:

- Endurance problem
- Performance w.r.t. DRAM
- Energy consumption increases
NVRAM as working memory

- CPU
- NVRAM
- Disk

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NVRAM as working memory

Existing works with PCM:

- Endurance problem
- Performance w.r.t. DRAM
- Energy consumption increases
NVRAM as the only memory
NVRAM as the only memory

CPU ➔ DRAM ➔ NVRAM ➔ Disk

Impact on the implementation (Harvard/Von Neumann architecture)
NVRAM as the only memory

- Impact on the implementation (Harvard/Von Neumann architecture)
Operating system

- Paging...

Diagram:
- CPU
- MMU
- TLB
- Page table (in RAM)
- DRAM
  - Frame 0
  - Frame 1
  - Frame 2
  - Frame 3
  - Frame 4
  - Frame 5
  - …
  - Frame n
Operating system

- Paging...
- ...vs. file system
Operating system: boot and reboot?

- Installation and launch

Diagram:
- CPU
- DRAM
- Disk

No reboot... bug? reset? Checkpoint?

Compilation
- produce new executable files
- decides when to checkpoint?
Operating system: boot and reboot?

- Installation and launch

CPU → DRAM → Disk

- ELF header
- Program header table
- .text
- .rodata
- ...
- .data
- Section header table

No reboot... bug? reset? Checkpoint?

Compilation produces new executable files.

decides when to checkpoint?
Operating system: boot and reboot?

- Installation and launch

CPU

DRAM

Disk

ELF header

Program header table

.text

.rodata

...

.data

Section header table
Operating system: boot and reboot?

- Installation and launch

![Diagram]

- CPU
- DRAM
- NVRAM
- Disk
Operating system : boot and reboot ?

- Installation and launch

- No reboot...
  - bug ?
  - reset ? Checkpoint ?

- Compilation
  - produce new executable files
  - decides when to checkpoint ?
Programming model

- With DRAM + Disk: decide what is persistent
- With NVRAM: decide what is non-persistent
Peripherals

- Flash memory
- RTC
- Magnetometer
- Accelerometer
- Barometer
- Hydrometer&Thermometer
- Lightmeter
- PIR
- FRAM memory
- Energy harvesting
- Reset button
- 2xAA/Li-Ion
Glory?

Test my ideas, publish, be famous
Glory?

Test my ideas, publish, be famous

Buy a computer that includes MRAM
Glory?

Test my ideas, publish, be famous

Buy a computer that includes MRAM
Simulation ;-(
Simulation ;-)

- Not so bad
Simulation ;-(*

- Not so bad
  - Explore memory hierarchies
  - Feedback to architects
- Extrapolate from dram accesses: No!
- Emulate: yes (but not so easy)
Which technology?

- Which technology is realistic?
- Understand the technology
Which technology?

- Which technology is realistic?
- Understand the technology

Keywords:
- TaOxprocess
- Damascene
- TiOx
- lithography
- CMOS
- SiOx
- nanoimprintratio
- substrate
- layer
- ON/OFF
What about us?

- Internet of Things
- Energy harvesting
Why now ?

- Because architects will (again) design CPUs impossible to program
  - ...or we can help design these CPUs
- Lots of recent works
- Real platform appeared recently
Conclusion

- Can lead to huge changes in computer science
- Simulation necessary, for now
- Feedback to architects
- Memory hierarchy depends on the use case
- Which technology is viable?
  - Always in motion the future is...
Credits

- **Bibliography**: kevinmarquet.net/research/nvram
- **Pictures**:
  - Small bib: andrebourgeois.fr/ImageBibliotheque.JPG
  - Big bib: www.10escadron.com/bibliotheque/
  - Rolex: blog.titanblack.co.uk/wp-content/uploads/2013/04/Platinum-Rolex-Daytona-Basel-2013.jpg
  - Elf: www.johnloomis.org/microchip/pic32/elf/Elf-layout.png
  - Key: http://www.businesshi-lite.co.za/wp-content/uploads/2012/06/key-small-1024x768.jpg
  - Sensor: www.libelium.com/libelium-images/generico/waspmote_radiation_sensor_board-1000.png
  - Wislab: wislab.cz/media/content-images/WislabNode-S-description.png
  - Simulation: www.mpg.de/698541/standard.jpeg
Backup: fetch-decode-execute