CMOS TRANSISTOR: FDSOI VS. FINFET

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MOORE’S LAW IS DEAD: EVERYTHING IS POSSIBLE

Metal-Oxide-Semiconductor (MOS): smallest brick of advanced electronic devices

Scaling-down dimensions (=node) enabled improvement of:

- Performance
- Power
- Area
- # of transistors per $:

Till the 28nm node. Below => technology complexity
BEYOND THE WALL: FULLY-DEPLETED AND SUB-28NM CMOS TECHNOLOGY

- finFET at 22nm node (INTEL, 2011)
- FDSOI at 28nm node (STMicroelectronics, 2012)
OUTLINE

1 The Fully Depleted solution
2 FDSOI and FDSOI momentum
3 finFET
4 FDSOI vs. finFET
5 Conclusion
Below 28nm: electrostatic limits (Gauss)

PMOS, 20nm from IBM (Shang et al., VLSI’12)
The last bulk (=non fully-depleted) technology
“FULLY DEPLETED”: ELECTROSTATIC BOOSTER

- Depletion: no free carriers, only negative ions. Then electron channel

- Depletion:
  - detrimental to switch quickly from OFF-state to ON-state
  - Induce parasitic coupling between drain and channel

- Depletion region should be reduced

=> the Fully Depleted solution

*PMOS, 20nm from IBM (Shang et al., VLSI’12)
The last bulk (=non fully-depleted) technology*
Fully-Depleted (FD) devices are the solution for low voltages (= low power)

<table>
<thead>
<tr>
<th>Vdd (V)</th>
<th>Speed Gain</th>
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<tbody>
<tr>
<td>0.6</td>
<td>84%</td>
</tr>
<tr>
<td>0.7</td>
<td>62%</td>
</tr>
<tr>
<td>0.8</td>
<td>49%</td>
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<tr>
<td>0.9</td>
<td>38%</td>
</tr>
<tr>
<td>1</td>
<td>32%</td>
</tr>
<tr>
<td>1.1</td>
<td>29%</td>
</tr>
<tr>
<td>1.2</td>
<td>27%</td>
</tr>
</tbody>
</table>

N. Planes et al., 28nm FDSOI, VLSI’12
TODAY EVERYONE FEELS “FULLY DEPLETED”

FD-SOI

finFET

and others
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2. FDSOI and FDSOI momentum
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MIGRATION TOWARDS FDSOI: REQUIREMENTS

Some FDSOI features / requirements:

- High-k / metal gate stack for OFF-state current
- Raised sources/drains for low parasitic access resistance
- Buried Oxide thickness: $T_{\text{BOX}} \approx 25-20\text{nm}$
- Channel thickness: $T_{\text{si}} \approx 7-6\text{nm}$ (key dimension for electrostatics)

Legacy from 28-20nm node

PMOS, 20nm from IBM (Shang et al., VLSI'12)

SOI-substrate

M. Haond et al., S3S’14, 20nm node
Substrate is ready:

- Availability: SOITEC with second source with Shin-Etsu and agreement with SunEdison (former MEMC)
- Performance
  - Roughness below 2A RMS
  - Uniformity: +/- 5A total thickness variation on a 300mm wafer
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Finfet is a new “animal”
- Highly 3D
- With the depletion region limited by the gate itself in the width direction
- Benefiting from a double gate control

Source: Intel
- Quantized current (by # of fins in //) => SRAM & analog constraint => less flexibility

- More current/surface unit => thermal issues
FINFETS W/ REPLACEMENT GATE

finFET with replacement gate (=gate-last =damascene); with drawbacks:

- Scalability
- Parasitic capacitance
- Parasitic (gate) resistance: detrimental for Radio Frequency RF applications
- Process complexity (3D + replacement gate)
1. The Fully Depleted solution
2. FDSOI and FDSOI momentum
3. finFET
4. FDSOI vs. finFET
   • Technology
   • Scaling paths
   • Design considerations
5. Conclusion
FDSOI is scalable by scaling of:

- Thickness $\downarrow$ (electrostatics)
- Width $\downarrow$ (density)
- Strain $\uparrow$ in high mobility channels (performance)

Because current increases w/ strain

$T_{si} = L/4$

$W_{fin} = L/2$

M. Haond et al., S3S’14, 20nm node
finFET is scalable by scaling of:

- width ↘ (electrostatics)
- pitch ↘ (density)
- height ↑ (performance)

Because current proportional to effective width; being $W_{\text{eff}} = 2.H_{\text{fin}} + W_{\text{fin}}$
- Current is proportional to $W_{eff}=2H_{fin}+W_{fin}$. To be compared w/ the fin pitch (=planar case)
  - 22nm node => + 28% gain
  - 14nm node => + 119% gain
- SRAM and dense cells directly benefits from this geometrical 3D-induced gain

0.0588 $\mu$m² SRAM 14nm finFET
0.54x vs. 22nm finFET

Source: Intel
- finFET current $I \sim W_{\text{eff}}$ ... but gate capacitance $C \sim W_{\text{eff}}$

- High density
- Low-cost

\begin{aligned}
\text{gate} & \quad \equiv \quad \text{fan-out} \\
\text{FDSOI} & \quad \text{node 28nm} \\
& \quad \text{Low-cost}
\end{aligned}

\begin{aligned}
\text{gate} & \quad \equiv \quad \text{fan-out} \\
\text{finFET} & \quad \text{node 22nm} \\
& \quad \text{High density}
\end{aligned}
BACK BIASED CAPABILITY

- Capability to increase or reduce current with back (=substrate) bias
- Already existed on bulk. Not efficient on FinFETs but **highly efficient on FDSOI**
- **Flexibility for designers:**
  - to compensate electrical fluctuations
  - to increase speed or reduce power **ON-DEMAND**
High Back-Bias efficiency means Low Dynamic Power:

- **Dissipated power divided by 2 at same frequency**
- Interesting for both low-voltage Internet-of-Things (IoT) and high-end high-perf applications (US data-centers = 5 power plants = 5 millions of houses)

**THE GREAT ADVANTAGE OF FDSOI VS. FINFET**
POWER EFFICIENCY: FDSOI VS FINFET

- finFET can deliver more performance
- FDSOI can achieve less total power
- FDSOI covers a wider window of Performance/Power
- Back-gate bias allows “performance-on-demand” and “power efficiency”

Cortex-A32/A35 cores

Will Abbey, 2016

Source: SOIconsortium
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CONCLUSIONS

- Some applications need **more** digital, more density and more performance
- Others need **less** power, low-cost, more sensing (analog), more connectivity (RF), more flexibility, more energy efficiency and more reliability (radiation tolerance for automotive and space)
- finfet and planar FDSOI fulfill different requirements for different applications

**FDSOI vs. FINFET => FDSOI AND finFET**
CMOS ROADMAP

Energy efficiency (GOPS/mW)

Low Power Applications
Low leakage low-power device for IOT

High Performance digital
HPC applications

Performance (GOPS)
Merci
Leti, **50** years of pioneered innovations

Leti Day, **2** days of discovery, innovation & networking

Leti Gala Evening, **1** VIP Event for our partners & prospects